REMARKS

A. Drawing Objections

The drawings were objected to under 37 CFR 1.83(a). The Examiner has objected that the drawings do not show multiple levels of SONOS transistors formed above one another. Fig. 3b has accordingly been amended to include indication of an additional SONOS memory level formed above the memory cell shown in Fig. 3b. A replacement drawing sheet is included with this response. This drawing amendment is a simple restatement of material found in paragraph [0058], and does not constitute new matter.

B. Status of the Claims

Claims 1-59 are pending in the application. Claims 1-9, 11, 12, 15, 16, 18-25, 27, 28, 31-41, and 43-53 were rejected under 35 USC 102(e) as being anticipated by Muria et al., US Patent No. 6,469,343. Claims 1 and 17 were rejected under 35 USC 102(e) as being anticipated by Muria et al. Claims 10, 42, and 48 were rejected under 35 USC 103(a) as being unpatentable over Miura et al. in view of Chan et al., US Patent No. 6,797,604. Claims 13, 14, 26, 29, and 40 were rejected under 35 USC 103(a) as being unpatentable over Miura et al. in view of Paton et al., US Patent No. 6,682,973. Claims 54-59 were rejected under 35 USC 103(a) as being unpatentable over Miura et al. in view of Lee et al., US Patent Publication No. 2002/0028541.

C. 35 USC 102(e) Claim Rejections: Claims 1-9, 11, 12, 15, 16, 18-25, 27, 28, 31-41, and 43-53

Claims 1-9, 11, 12, 15, 16, 18-25, 27, 28, 31-41, and 43-53 were rejected under 35 USC 102(e) as being anticipated by Muria et al. Of these claims, claims 7, 23, 27-28, 31-32, 39, 51, and 53 have been cancelled.

As amended, claim 1 recites a SONOS-type device comprising: a tunneling dielectric, a dielectric charge storage layer in contact with the tunneling dielectric, the charge storage layer comprising a first dielectric film and a second dielectric film, wherein the first and the second dielectric films are formed of different materials; a blocking dielectric in contact with the charge storage layer; and a semiconductor channel region in contact with the tunneling dielectric, wherein the semiconductor channel region comprises polysilicon.

It is conventional to form channels of semiconductor memory devices in a wafer surface; i.e. in monocrystalline silicon, not in polycrystalline silicon as in the claim. There is no teaching in Miura et al. that the channel region (C of Fig. 1) of Miura et al. is polysilicon, or that the device is a thin film transistor device. Thus claim 1 and its dependent claims distinguish over the device of Miura et al.

As will be discussed further in section F addressing the 35 USC 103 rejections of claim 13, 14, 26, 29, and 30 (over Miura et al. in view of Paton et al.) the device of claim 1 is not suggested by the cited references or any combination thereof.

The other independent claims included in this rejection were claims 18, 33, 38, and 47, all of which, as amended, also recited a polysilicon channel, and thus distinguish over Miura et al. using the same rationale.

Claims 18 and 47 including the additional limitation that the memory cell is in a monolithic three dimensional memory array, thus distinguishing them further.

Applicants respectfully request reconsideration of the 35 USC 102(e) rejections of claims 1-6, 8-9, 11, 12, 15, 16, 18-22, 24-25, 33-38, 40-41, 43-50, and 52.

D. 35 USC 102(e) Claim Rejections: Claims 1 and 17

Claims 1 and 17 were rejected under 35 USC 102(e) as being anticipated by Muria et al. As noted in section C, the device of claim 1, as amended, includes a polycrystalline channel, which is neither taught nor suggested by Miura et al.

Reconsideration is respectfully requested.

E. 35 USC 103(a) Claim Rejections: Claims 10, 42, and 48

Claims 10, 42, and 48 were rejected under 35 USC 103(a) as being unpatentable over Miura et al. in view of Chan et al.

Claim 10 depends from claim 1. As addressed in prior sections, the device of claim 1, as amended, includes a polycrystalline channel, which is neither taught nor suggested by Miura et al.

Claim 42 depends from claim 38, and claim 48 depends from claim 47. Claims 38 and 47 have similarly been amended to recite a device having a polysilicon channel, and thus claims 42 and 48 are neither taught nor suggested by the combination of Miura et al. an Chan et al.

Reconsideration is respectfully requested.

F. 35 USC 103(a) Claim Rejections: Claims 13, 14, 26, 29, and 30

Claims 13, 14, 26, 29, and 30 were rejected under 35 USC 103(a) as being unpatentable over Miura et al. in view of Paton et al.

Claims 13 and 14 have been cancelled, their limitations included in claim 1. Claim 1 recites a SONOS-type device comprising a tunneling dielectric, a dielectric charge storage layer in contact with the tunneling dielectric, the charge storage layer comprising a first dielectric film and a second dielectric film, wherein the first and the second dielectric films are formed of different materials; a blocking dielectric in contact with the charge storage layer; and a semiconductor channel region in contact with the tunneling dielectric, wherein the semiconductor channel region comprises polysilicon.

The Examiner notes that Miura et al. do not disclose a channel made of polysilicon. The Examiner points out that Paton et al. does so, and asserts:

> It would have been obvious to one having ordinary skill in the art at the time the invention was made to be within the general skill of a worker in the art to select known material on the basis of its suitability for the intended use as a matter of design choice.

As the Examiner will surely know, however, it was in no way conventional at the time of filing of the present application to form TFT arrays of SONOS memory cells. TFT arrays, built having a channel region formed in polysilicon rather than in a monocrystalline silicon wafer, have been used almost exclusively in flat panel displays. The TFT device of a flat panel display is not a memory device, and has no charge storage region. Such a device is merely required to have an "on" state and an "off"state. The requirements for a memory cell, however, are more stringent. The memory cell must hold a memory state based on the presence or absence of charge stored in a charge storage region. The stored charge affects the threshold voltage of the transistor, the voltage at which it turns on, allowing its memory state to be sensed.

Due to the more stringent requirements of a memory cell, polysilicon would not be routinely selected by one skilled in the art; conventional knowledge would deem

polysilicon unsuitable for this material for the intended use. This choice is in no way obvious.

G. 35 USC 103(a) Claim Rejections: Claims 54-59

Claims 54-59 were rejected under 35 USC 103(a) as being unpatentable over Miura et al. in view of Lee et al.

Claim 54 recites a memory cell comprising: a channel region; and a tunneling oxide grown by an in situ steam generation process, the tunneling oxide in contact with the channel region, wherein the memory cell is a portion of a monolithic three dimensional memory array comprising at least two levels of memory cells, one level formed vertically over the other.

The Examiner notes that Miura et al. "is silent on the memory array having two levels of SONOS-type memory cells, where one level is formed on top of the other." The Examiner points to Lee et al. for this teaching, and continues:

> It would have been obvious to one skilled in the art to arrange the memory cell arrays on top of eachother for the mere convenience of spatial conservation and larger memory capacity, which has been the leading trend in semiconductor technology ...

There is no motivation found in the references to combine them. MPEP 2143 describes the basic requirements of a *prima facie* case of obviousness:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
>
> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.

There is no suggestion in Miura et al. to form its monocrystalline device as a multiple levels of TFT devices, nor is there any suggestion in Lee et al. that improvements in retention warrant increasing process complexity to change the device. The Examiner has not identified any such suggestion.

Applicants respectfully believe that the Examiner has not established a *prima facie* case of obviousness, and request reconsideration.

CONCLUSION

In light of this response, Applicants believe this application to be in condition for allowance. If there are any questions concerning this response, the Examiner is invited to contact the undersigned agent at (408) 869-2921.

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Respectfully submitted,

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